THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY | DEPARTMENT OF ELECTRONIC & COMPUTER ENGINEERING

Design and Fabrication of Resistive RAM for AI Circuits (CM03)

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Introduction

Background

- Memory technologies such as SRAM, DRAM, and FLASH are widely used for cache, main memory, and solid-state drives today. However, these technologies are based on charge storage mechanisms and face challenges in scaling down to 10nm or below, leading to performance degradation and increased power consumption.
- Resistive random access memory (RRAM) is considered a strong contender of the next-generation memory technology. It operates differently from charge-based memory technologies by relying on the formation and rupture of conductive filaments in the insulator between two electrodes to store data.
- To achieve a memory array and minimize the sneak path current, the form of one-transistor one-RRAM (1T1R) configurations is more preferred. Although the dimension of the one-diode one-RRAM (1D1R) array is smaller, the 1T1R architecture has a lower sneak path current, because the transistor limits the current flowing through the non-selected RRAM cell by controlling the gate voltage.
- Thin-film transistors (TFTs) are better suited for the 1T1R devices since they have a simpler structure, lower processing temperature and fewer fabrication processes.
- Due to a higher field-effect mobility, lower off-state current, better uniformity, and lower process temperature, amorphous indium-gallium-zinc oxide (a-IGZO) is used as the channel of the TFT devices.
- To simplify the fabrication process and reduce the mask cost, separate device fabrication is applied. After the fabrication, the a-IGZO EMMO TFT devices and RRAM cells are connected through wire bonding.

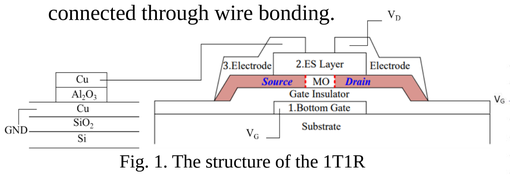

Fig. 1. The structure of the 1T1R

Objectives

- To design the layout and structure of the 1T1R
- To fabricate the TFT devices and RRAM cells
- To connect the fabricated devices
- To characterize the fabricated devices

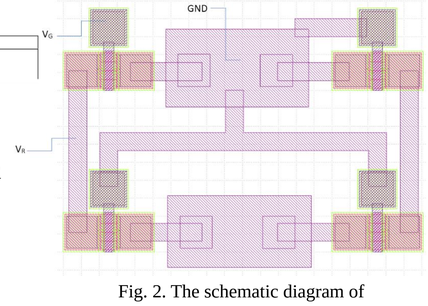

Fig. 2. The schematic diagram of the 2x2 1T1R memory array

Hypothesis

- In a 1T1R configuration memory array, the TFT devices can effectively reduce the sneak path current since the current flowing through the unselected RRAM cell is limited by the transistor with a grounded gate voltage.

Experiment

- We fabricated a-IGZO EMMO TFT devices and Cu/ Al_2O_3/Cu RRAM cells.
- We formed a TFT/RRAM hybrid device and 1T1R memory array through wire bonding.

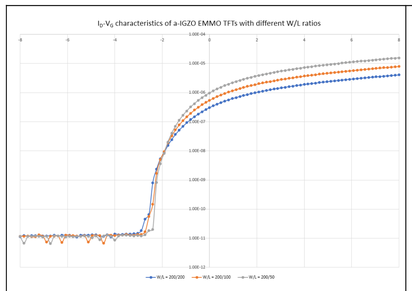

Fig. 3. I_D-V_G characteristics of the a-IGZO EMMO TFT devices with different W/L ratios

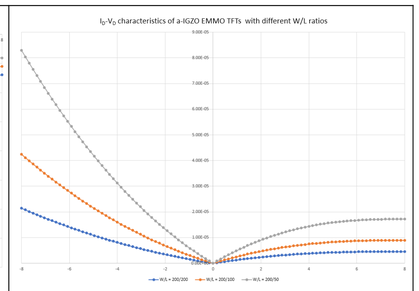

Fig. 4. I_D-V_D characteristics of the a-IGZO EMMO TFT devices with different W/L ratios

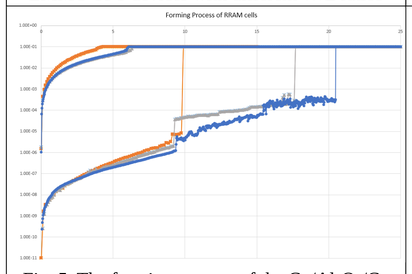

Fig. 5. The forming process of the Cu/Al_2O_3/Cu devices with 5nm, 10nm and 15nm Al_2O_3

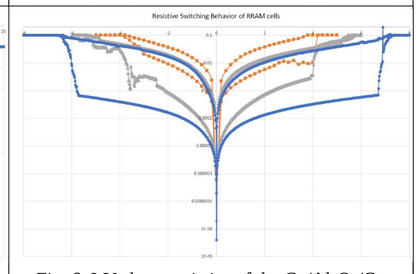

Fig. 6. I-V characteristics of the Cu/Al_2O_3/Cu devices with 5nm, 10nm and 15nm Al_2O_3.

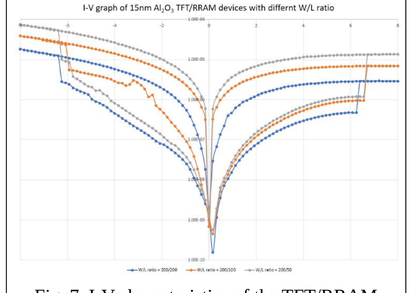

Fig. 7. I-V characteristics of the TFT/RRAM hybrid devices with 15nm Al_2O_3, and different W/L ratios.

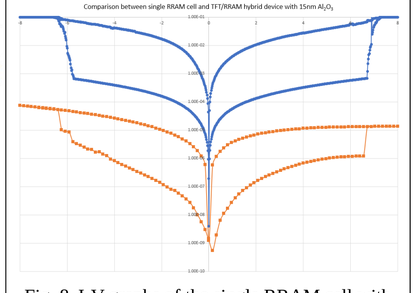

Fig. 8. I-V graphs of the single RRAM cell with 15nm Al_2O_3 and the TFT/RRAM hybrid device with 15nm Al_2O_3 and 200/500 W/L ratio.

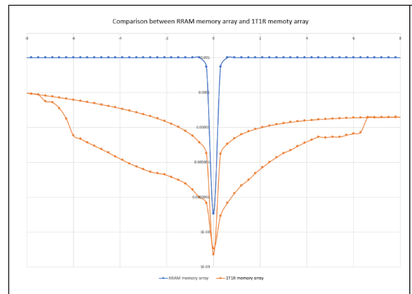

Fig. 9. I-V graphs of the RRAM memory array with 15nm Al_2O_3 and 1T1R memory array with 15nm Al_2O_3 and 200/50 W/L ratio.

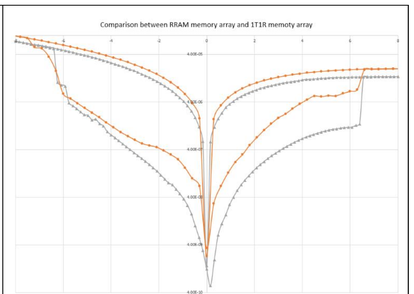

Fig. 10. I-V graphs of 1T1R array with 15nm Al_2O_3 and 200/50 W/L ratios and the hybrid device with 15nm Al2O3 and 200/500 W/L ratio.

From Fig. 9, when the voltage (V_R) of 2V is applied, t**he on/off ratio of the 1T1R array** is estimated at about **14.2**.

Shown in Fig.9, predictably, the RRAM memory array cannot store data because of the sneak path current problem. In both LRS and HRS case, the measured current is 1mA, which is the compliance current. On the other hand, in the 1T1R memory array, thanks to the switching capability of **TFT**, it **limits current flowing through unselected cells**. So, most current flows through the selected cell, so a lower HRS resistance value is obtained. Hence, the 1T1R memory array exhibit memory behavior, and the sensor amplifier **can distinguish LRS and HRS** during read operation.

When comparing with the TFT/RRAM hybrid device through Fig. 10, the most obvious changes are the current value in both LRS and HRS. In both states, there is an increase in current which is regarded as the current flowing through unselected cells. The existence of the parallel resistance reduces the on/off ratio, so it is reasonable to obverse that the on/off ratio of the 1T1R memory array is smaller than that of the TFT/RRAM hybrid device.

Conclusion

- Our work has demonstrated t**he method to reduce the sneak path current in a RRAM memory array**. In a 1T1R setup, we observe that **the TFT with higher output current capability is more suitable for the construction of the RRAM memory array**, resulting in a more accurate HRS/LRS discrimination capability. After implementing the TFT in the 2x2 RRAM array, the 1T1R memory array possesses memory behavior, with 14.2 on/off ratio. The reduction of sneak path current can significantly minimize errors in the read operation.
- However, retention time and endurance tests should be further analyzed, such that the memory behavior in a RRAM cell will be analyzed more comprehensively.
- The findings presented in this work have the potential to enable the realization of more tightly packed memory architecture by implementing the 1T1R architecture.